Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025

Third Semester

Electronics and Communication Engineering

UECTL24301 - Digital Systems Design

Regulations - 2024

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BTL*	*CO*	*Marks*
1.	Convert $A3B_H$ into Binary.	L3	1	2
2.	Implement Using NAND gates only F=xyz+x'y'.	L2	1	2
3.	Differentiate between half adder and full adder.	L2	2	2
4.	Mention the applications of Decoder.	L2	2	2
5.	Write the excitation table for SR FF.	L2	3	2
6.	List the types of flip-flop.	L2	3	2
7.	Distinguish between synchronous and asynchronous sequential circuits.	L2	4	2
8.	Compare critical and non-critical race.	L2	4	2
9.	What are the characteristics of TTL logic?	L2	5	2
10.	Define Fan-In and Fan-Out.	L2	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a		Simplify the Minimized logic function using K-Maps. F (A, B, C, D) = ∑m (1,3,5,8,9,11,15)+ ∑d(2,13). Implement the minimal SOP using NAND and NOR gates.	L3	1	16
			Or			
	b		Obtain (i) Sum of products form and (ii) Product of sums form for F=x'z'+y'z'+yz'+xy.	L3	1	16
12.	a	i	Implement the following Boolean function F= ∑m (0,3,5,8,9,10,12,14). using 8:1 Mux.	L3	2	8
		ii	Design a 2-bit magnitude comparator.	L3	2	8
			Or			
	b	i	Design logic diagram for 1 of 8 demultiplexer.	L3	2	8
		ii	Design 4 to 16 line decoder can be built using 2 to 4 line decoder.	L3	2	8

13.	a	i	Realize SR flip-flop using D flip-flop and JK flip-flop.	L3	3	8
		ii	Compare Synchronous and Ripple counters.	L3	3	8
			Or			
	b	i	Design and implement Mod-10 Synchronous Up counter using T-FFs.	L3	3	8
		ii	Determine the characteristic table, Truth table, characteristic equation and excitation table for T FF.	L3	3	8
14.	a	i	Design an asynchronous sequential circuit that has two inputs X2 and X1 and one output Z. When X1=0, the output Z is 0. The first change in X2 that occurs while X1 is 1 will cause output Z to be 1. The output Z will remain 1 until X1 returns to 0.	L4	4	8
		ii	Explain the process of state reduction in asynchronous sequential circuit with an example?	L2	4	8
			Or			
	b	i	Explain the fundamental & pulse mod asynchronous sequential circuit.	L2	4	8
		ii	Construct hazard free realization for the following Boolean function. F (A, B, C, D) = ∑m (1,5,6,7) using AND- OR gate network.	L4	4	8
15.	a		Design the following sum-of-minterms using PAL. W(A,B,C,D)=∑(2,12,13) X(A,B,C,D)=∑(7,8,9,10,11,12,13,14,15) Y(A,B,C,D)=∑(0,2,3,4,5,6,7,8,10,11,15) Z(A,B,C,D)=∑(1,2,8,12,13).	L4	5	16
			Or			
	b		With neat diagram, explain the operation of CMOS NAND and NOR gates.	L2	5	16